

1 1. (Amended) A memory system comprising:
2 a memory controller having an interface that includes a
3 plurality of memory subsystem ports;
4 a first memory subsystem including:
5 a buffer device having a first port and a second port,
6 and
7 a plurality of memory devices coupled to the buffer device
8 via the second port, wherein data is transferred between at
9 least one memory device of the plurality of memory devices and
10 the memory controller via the buffer device;
11 and
12 a plurality of point-to-point links, each point-to-point link
13 of the plurality of point-to-point links having a connection to a
14 respective memory subsystem port of the plurality of memory
15 subsystem ports, the plurality of point-to-point links including a
16 first point-to-point link to connect the first port to a first
17 memory subsystem port of the plurality of memory subsystem ports.

1 2. (Amended) The memory system of claim 1 further including:
2 a plurality of connectors, wherein each connector of the
3 plurality of connectors is connected to a respective point-to-point
4 link of the plurality of point-to-point links; and
5 a plurality of memory subsystems, and wherein each memory
6 subsystem of the plurality of memory subsystems includes:
7 a buffer device having a first port and a second port,
8 wherein the first port is coupled to a respective connector of

9 the plurality of connectors; and

10 a plurality of memory devices coupled to the buffer
11 device via the second port.

1 3. (Amended) The memory system of claim 2 further including
2 a plurality of substrates wherein each memory subsystem of the
3 plurality of memory subsystems is disposed on a respective substrate
4 of the plurality of substrates.

1 4. (Amended) The memory system of claim 1 wherein the plurality
2 of point-to-point links, first memory subsystem, and memory
3 controller are disposed on a common substrate.

1 5. (Amended) The memory system of claim 1 wherein the first
2 memory subsystem further includes a plurality of channels and a
3 plurality of memory device select lines connected between the
4 plurality of memory devices and the second port.

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B1 1 6. The memory system of claim 5 wherein each channel includes
2 a plurality of terminated signal lines.

1 7. (Amended) The memory system of claim 1 wherein the buffer
2 device of the first memory subsystem further includes a clock
3 alignment circuit to generate an internal synchronizing clock signal
4 having a predetermined timing relationship with a reference clock
5 signal.

1 8. (Amended) The memory system of claim 1 further including
2 a plurality of sideband signals coupled between the plurality of
3 memory devices of the first memory subsystem and the memory

4 controller.

Sub B2 9. (Amended) The memory system of claim 1 further including
2 a plurality of sideband signals coupled between the plurality of
3 buffer devices and the memory controller.

Q 10. (Amended) A memory system comprising:
2 a controller device;
3 a first buffer device having a first interface and a second
4 interface;
5 a second buffer device having a first interface and a second
6 interface;
7 a first point-to-point link having a first connection to the
8 controller device and a second connection to the first interface of
9 the first buffer device;
10 a first plurality of memory devices connected to the second
11 interface of the first buffer device;
12 a second point-to-point link having a first connection to the
13 controller device and a second connection to the first interface of
14 the second buffer device; and
15 a second plurality of memory devices connected to the second
16 interface of the second buffer device.

1 11. The memory system of claim 10, wherein the first buffer
2 device and first plurality of memory devices are disposed on a first
3 substrate, and the second buffer device and second plurality of
4 memory devices are disposed on a second substrate.

1 12. (Amended) The memory system of claim 11, further
2 including:

3 a first plurality of signal lines to connect the first
4 plurality of memory devices to the second interface of the first
5 buffer device;

6 a second plurality of signal lines to connect the second
7 plurality of memory devices to the second interface of the second
8 buffer device;

9 a first plurality of termination elements connected to the
10 first plurality of signal lines; and

11 a second plurality of termination elements connected to the
12 second plurality of signal lines.

1 13. The memory system of claim 10, wherein the first buffer
2 device further includes a third interface, the memory system further
3 including:

4 a third buffer device having a first interface and a second
5 interface;

6 a third point-to-point link having a first connection to the
7 third interface and a second connection to the first interface of
8 the third buffer device; and

9 a third plurality of memory devices connected to the second
10 interface of the third buffer device.

1 14. The memory system of claim 10 further including a third
2 point-to-point link having a connection to the controller and a
3 fourth point-to-point link having a connection to the controller.

1 15. (Amended) The memory system of claim 10 further including:

2 a first channel to connect the first plurality of memory
3 devices to the second interface of the first buffer device;

4 a second channel to connect the second plurality of memory
5 devices to the second interface of the second buffer device;

6 a third channel connected to the second interface of the first
7 buffer device;

8 a third plurality of memory devices electrically coupled to the
9 third channel;

10 a fourth channel connected to the second interface of the
11 second buffer device; and

12 a fourth plurality of memory devices electrically coupled to
13 the fourth channel.

1 16. The memory system of claim 15 further including:

2 a fifth and sixth channel connected to the second interface of
3 the first buffer device;

4 a fifth plurality of memory devices electrically coupled to the
5 fifth channel; and

6 a sixth plurality of memory devices electrically coupled to the
7 sixth channel.

1 17. The memory system of claim 10, further including at least
2 one termination element disposed on the first buffer device and
3 electrically connected to the first point-to-point link.

1 18. (Amended) The memory system of claim 10 wherein the first
2 and second buffer devices each further include a clock alignment

3 circuit to generate an internal synchronizing clock signal having
4 a predetermined timing relationship with a reference clock signal.

1 19. A memory system comprising:

2 a controller device;

3 a first and second plurality of buffer devices, each buffer
4 device of the first and second plurality of buffer devices having
5 an interface connected to a respective plurality of memory devices;

6 a first and second repeater device;

7 a first point-to-point link having a first connection to the
8 controller device and a second connection to the first repeater
9 device;

10 a second point-to-point link having a first connection to the
11 controller device and a second connection to the second repeater
12 device;

13 a first plurality of repeater links, each repeater link having
14 a first connection to a respective buffer device of the first
15 plurality of buffer devices, and a second connection to the first
16 repeater device; and

17 a second plurality of repeater links, each repeater link having
18 a first connection to a respective buffer device of the second
19 plurality of buffer devices and a second connection to the second
20 repeater device.

1 20. (Amended) The memory system of claim 19, wherein each
2 buffer device of the first and second plurality of buffer devices
3 and corresponding plurality of memory devices are each disposed on

4 one of a plurality of respective module substrates.

1 21. (Amended) The memory system of claim 19 further including
2 a third point-to-point link having an end connected to the
3 controller device and a fourth point-to-point link having an end
4 connected to the controller device.

21 1 22. (Amended) The memory system of claim 19 wherein each
2 buffer device of the first and second plurality of buffer devices
3 each further include a clock alignment circuit to generate an
4 internal synchronizing clock signal having a predetermined timing
5 relationship with a reference clock signal.

1 23. (Amended) A memory system comprising:
2 a controller device having an interface;
3 a first connector, second connector, and third connector;
4 a first point-to point link having a first connection to the
5 interface and a second connection to the first connector;
6 a second point-to-point link having a first connection to the
7 interface and a second connection to the second connector;
8 a third point-to-point link having a first connection to the
9 interface and a second connection to the third connector; and
10 a first memory subsystem including:
11 a buffer device connected to the first connector; and
12 a plurality of memory devices connected to buffer device,
13 wherein at least one memory device of the plurality of memory
14 devices transfer data to the controller device via the buffer
15 device.

21 1 24. (Amended) The memory system of claim 23 wherein the
2 second and third connectors support coupling to respective second
3 and third memory subsystems.

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Please **ADD** the following claims:

1 25. (New) The memory system of claim 1 further including a
2 second memory subsystem including:

3 a buffer device having a first port and a second port, wherein
4 the first port is connected to a second point-to-point link of the
5 plurality of point-to-point links; and

6 a plurality of memory devices coupled to the buffer device via
7 the second port.

20 1 26. (New) The memory system of claim 1 wherein each memory
2 device of the plurality of memory devices included in the first
3 memory subsystem includes a dynamic random access memory cell
4 array.

1 27. (New) The memory system of claim 1 further including a
2 module substrate having a connector interface, wherein the first
3 memory subsystem is disposed on the module substrate, and the
4 buffer device is electrically connected to the connector interface,
5 wherein the buffer device transceives data, control and address
6 signals between the plurality of memory devices and the connector
7 interface.

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1 28. (New) The memory system of claim 27 further including a
2 motherboard substrate having a socket which interfaces with the
3 connector interface, wherein the memory controller and the
4 plurality of point-to-point links are disposed on the motherboard
5 substrate.

1 29. (New) The memory system of claim 1 further including
2 first termination disposed on the buffer device and coupled to the
3 first point-to-point link, to terminate a first end of the point-
4 to-point link.

az 1 30. (New) The memory system of claim 29 further including
2 second termination disposed on the memory controller and coupled to
3 the first point to point link, to terminate a second end of the
4 point-to-point link.

1 31. (New) The memory system of claim 1 wherein the buffer
2 device communicates with the controller device over the first
3 point-to-point link by encoding symbols using a number of signal
4 levels, wherein the number of signal levels is greater than two.

1 32. (New) The memory system of claim 1 wherein the buffer
2 device further includes a cache memory coupled to the first port,
3 to store data being provided from the memory controller to at least
4 one memory device of the plurality of memory devices.

1 33. (New) The memory device of claim 1 wherein the buffer
2 device further includes a write buffer, coupled to the first port,

3 to hold data to be provided to at least one memory device of the
4 plurality of memory devices.

1 34. (New) The memory system of claim 10 wherein each memory
2 device of the first plurality of memory devices includes a dynamic
3 random access memory cell array.

1 35. (New) The memory system of claim 10 further including a
2 module substrate having a connector interface, wherein the first
3 buffer device is disposed on the module substrate, and the first
4 buffer device is electrically connected to the connector interface,
5 and wherein the first buffer device transceives data, control and
6 address information between the first plurality of memory devices
7 and the connector interface.

1 36. (New) The memory system of claim 35 further including a
2 motherboard substrate having a socket which interfaces with the
3 connector interface, wherein the controller device and the first
4 point-to-point link are disposed on the motherboard substrate.

1 37. (New) The memory system of claim 10 wherein the first
2 buffer device communicates with the controller device over the
3 first point-to-point link by encoding symbols using a number of
4 signal levels, wherein the number of signal levels is greater than
5 two.

1 38. (New) The memory system of claim 10 wherein the first
2 buffer device further includes a cache memory, coupled to the first
3 interface of the first buffer device, to store data being provided

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4 from the controller device to at least one memory device of the
5 first plurality of memory devices.

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B3 1 39. (New) The memory device of claim 10 wherein the first and
2 second buffer device further includes a write buffer, coupled to
3 the first interface of the first buffer device, to hold data to be
4 provided to at least one memory device of the first plurality of
5 memory devices.

Q 1 40. (New) The memory system of claim 19 wherein each buffer
2 device of the first and second plurality of buffer devices further
3 includes a cache memory to store data being provided from the
4 controller device to at least one memory device of the respective
5 plurality of memory devices.

1 41. (New) The memory device of claim 19 wherein each buffer
2 device of the first and second plurality of buffer devices further
3 includes a write buffer to hold data to be provided to at least one
4 memory device of the respective plurality of memory devices.

1 42. (New) The memory system of claim 23 wherein each memory
2 device of the plurality of memory devices included in the first
3 memory subsystem includes a dynamic random access memory cell
4 array.

1 43. (New) The memory system of claim 23 further including a
2 module substrate having a connector interface, wherein the first
3 memory subsystem is disposed on the module substrate, and the
4 buffer device is electrically connected to the connector interface,

5 and wherein the buffer device transceives data, control and address
6 signals between the plurality of memory devices and the connector
7 interface.

1 44. (New) The memory system of claim 43 wherein the first
2 connector is a socket which interfaces with the connector interface
3 and wherein the memory system further includes a motherboard
4 substrate, wherein the controller device, the socket, first, second
5 and third point-to-point links are disposed on the motherboard
6 substrate.

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1 45. (New) The memory system of claim 23 further including
2 first termination disposed on the buffer device to terminate a
3 first end of the point-to-point link.

1 46. (New) The memory system of claim 45 further including
2 second termination disposed on the controller device to terminate
3 a second end of the point-to-point link.

1 47. (New) The memory system of claim 23 wherein the buffer
2 device communicates with the controller device over the first
3 point-to-point link by encoding symbols using a number of signal
4 levels, wherein the number of signal levels is greater than two.

1 48. (New) The memory system of claim 23 wherein the buffer
2 device further includes a cache memory to store data being provided
3 from the controller device to at least one memory device of the
4 plurality of memory devices.

1 49. (New) The memory device of claim wherein the buffer
2 device further includes a write buffer to hold data to be provided
3 to at least one memory device of the plurality of memory devices.
